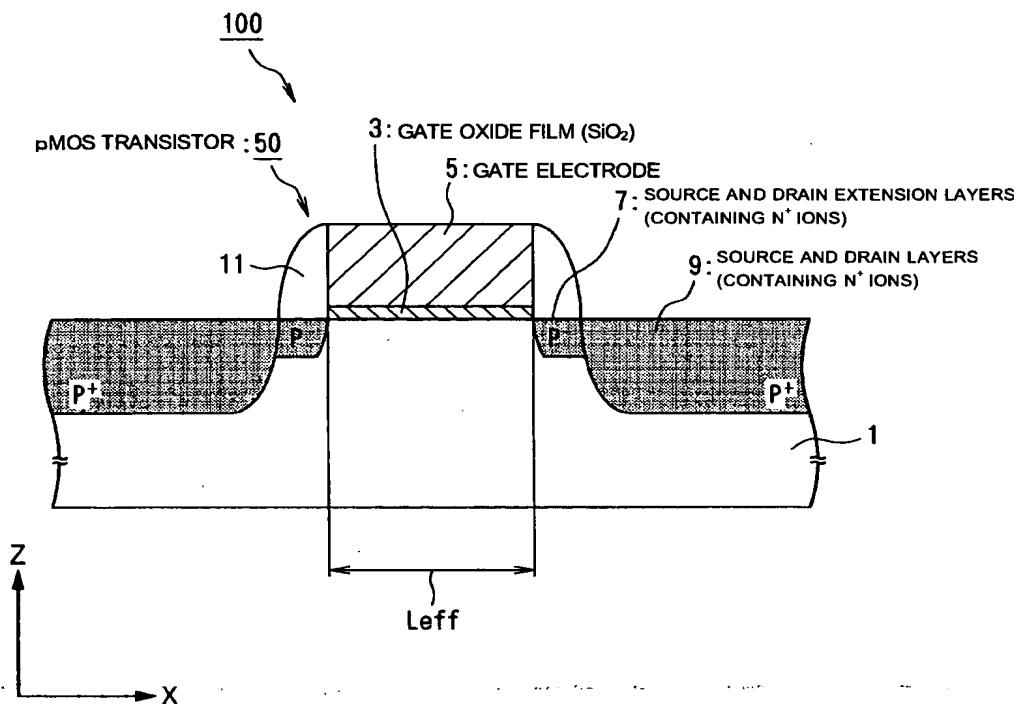
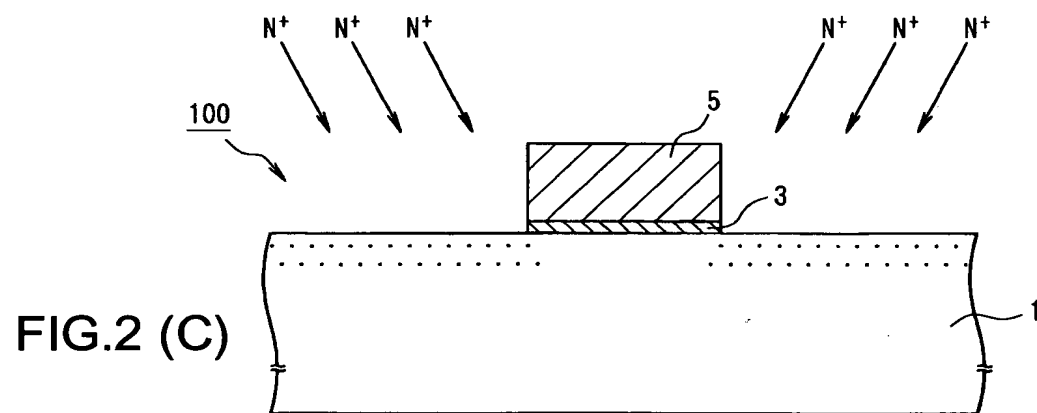
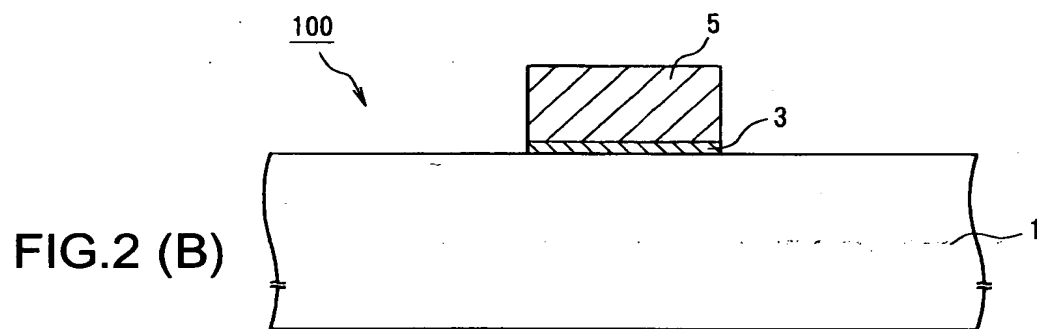
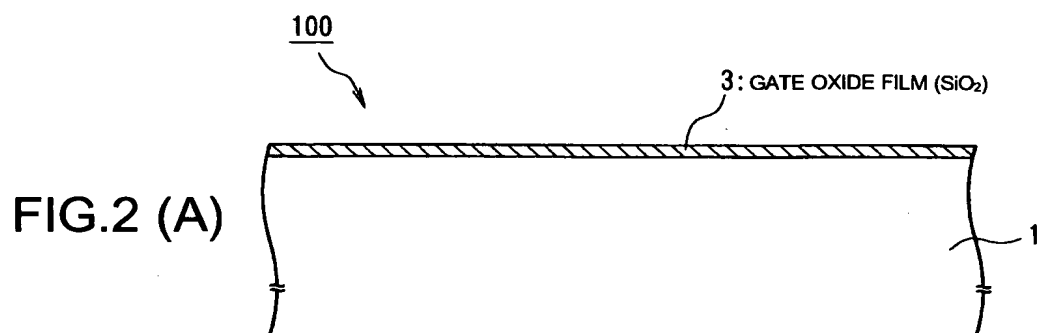


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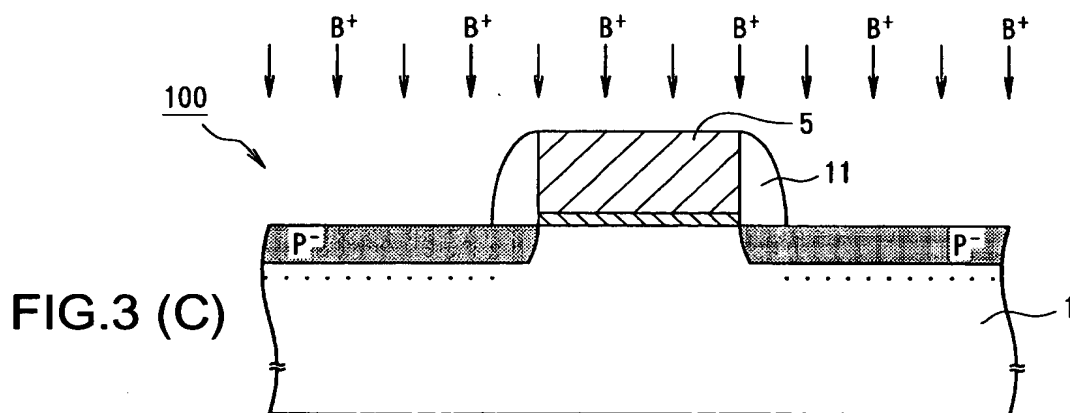
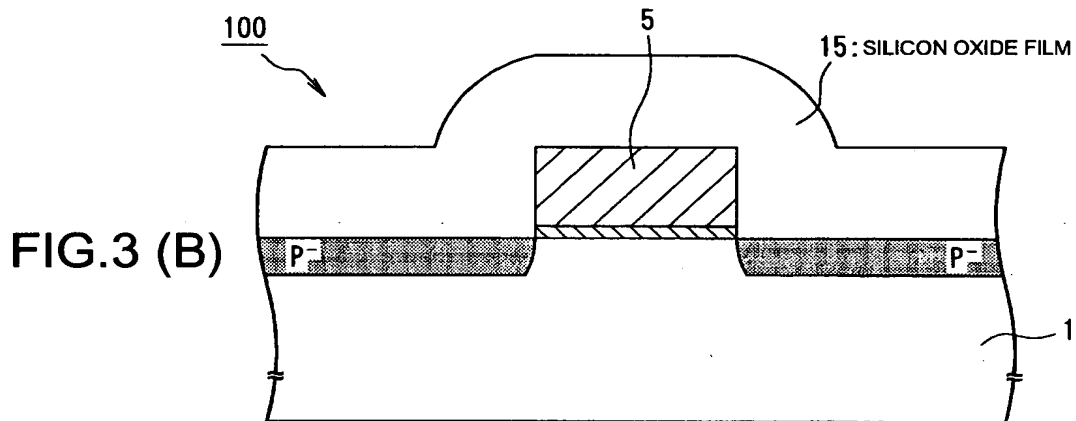
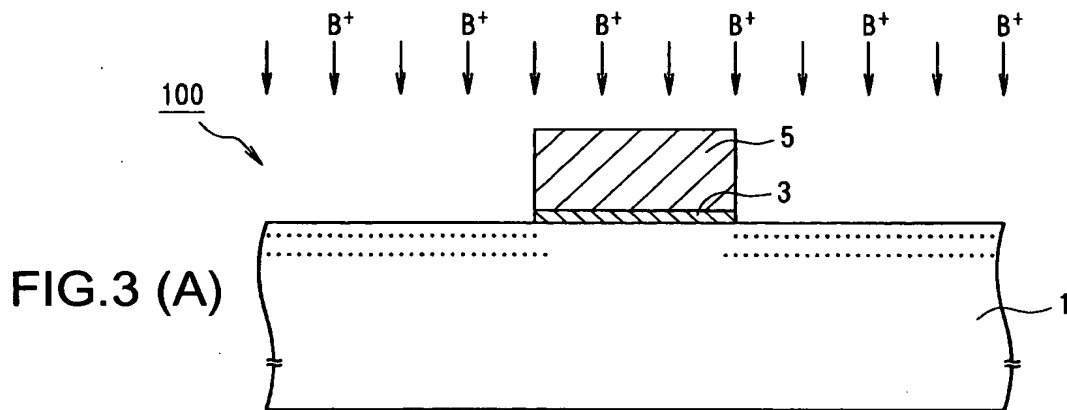
FIG.1



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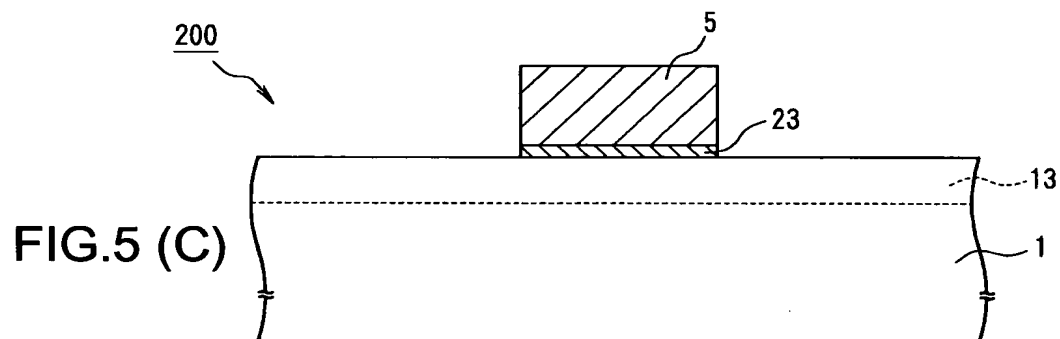
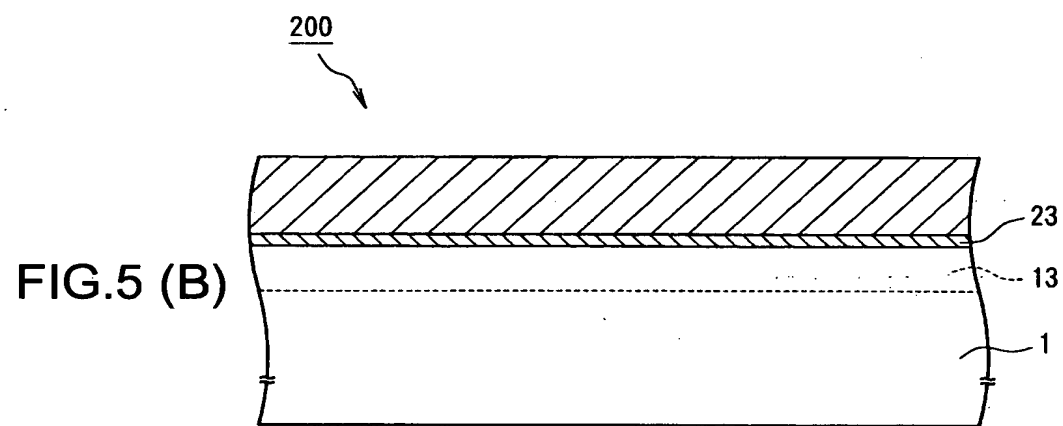
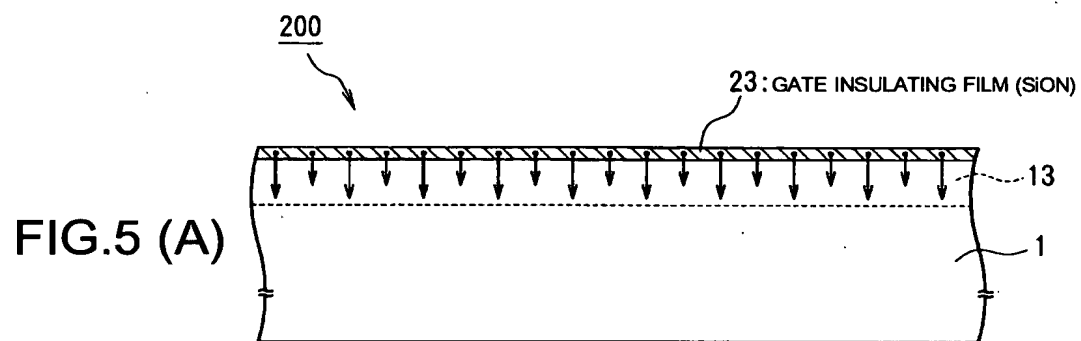


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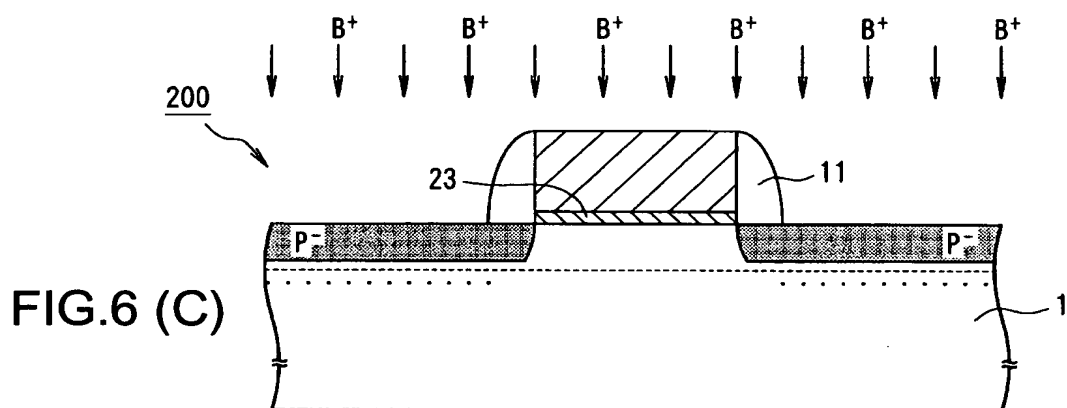
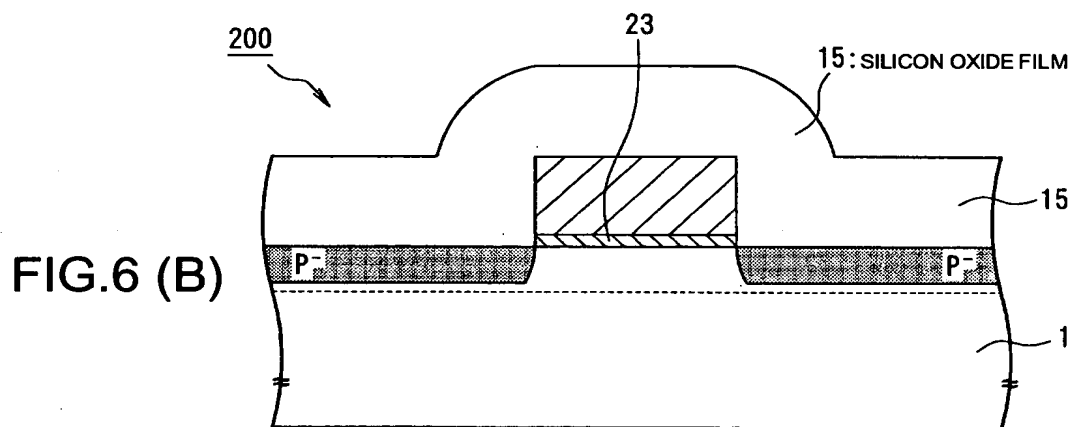
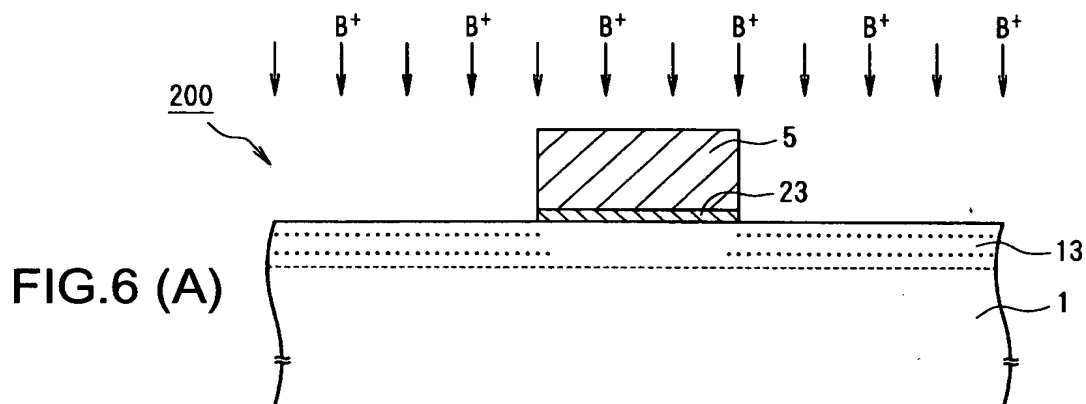


A cross-sectional view of a pMOS transistor 60 within a semiconductor device 200. The device is built on a substrate 1. A gate stack is formed on the surface, consisting of a gate insulating film 23 (SiON) and a gate electrode 5. The gate electrode 5 is surrounded by a gate sidewall 3. A p-type region 7 is formed in the substrate 1, adjacent to the gate stack. A p-type region 9 is formed in the substrate 1, adjacent to the p-type region 7. A p-type region 11 is formed in the substrate 1, adjacent to the p-type region 9. A p-type region 13 is formed in the substrate 1, adjacent to the p-type region 11. A dashed line indicates the boundary between the p-type region 13 and the p-type region 11. An arrow labeled X indicates the direction of the X-axis.

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FIG.7

